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Description generated with very high confidence

**Course Plan**

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| **Department :** | Computer Science and Engineering |
| **Course Name & code :** | COMPUTER ORGANIZATION AND ARCHITECTURE & CSE 2151 |
| **Semester & branch :** | THIRD & CSE |
| **Name of the faculty :** | DR. N. GOPALAKRISHNA KINI |
| **No of contact hours/week:** | |  |  |  |  | | --- | --- | --- | --- | | **L** | **T** | **P** | **C** | | 36 | 12 | 0 | 4 | |

**Course Outcomes (COs)**

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|  | ***At the end of this course, the student should be able to:*** | **No. of Contact Hours** | **Marks** |
| CO1: | Outline of Computer Hardware and Software, Methodology of machine instructions, addressing techniques and instruction sequencing. | 10 | 20 |
| CO2: | Relate typical components of EU, GPR, ALU Dedicated Hardware and their design to perform arithmetic operations. | 7 | 16 |
| CO3: | To understand the designing of the control unit. | 10 | 20 |
| CO4: | Describe about the basics of memory design, design of computer systems. | 10 | 20 |
| CO5: | Outline about the typical I/O techniques and describe the fundamental concepts of Parallel Architecture. | 11 | 24 |
|  | **Total** | 48 | 100 |

**Assessment Plan**

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| **Components** | **Assignments** | **Sessional Tests** | **End Semester/**  **Make-up Examination** |
| **Duration** | 20 to 30 minutes | 60 minutes | 180 minutes |
| **Weightage** | 20 % (4 X 5 marks) | 30 % (2 X 15 Marks) | 50 % (1 X 50 Marks) |
| **Typology of Questions** | Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation | Knowledge/ Recall; Understanding/ Comprehension; Application | Understanding/ Comprehension; Application; Analysis; Synthesis; Evaluation |
| **Pattern** | Answer one randomly selected question from the problem sheet (Students can refer their class notes) | MCQ: 10 questions (0.5 marks)  Short Answers: 5 questions (2 marks) | Answer all 5 full questions of 10 marks each. Each question may have 2 to 3 parts of 3/4/5/6/7 marks |
| **Schedule** | 4, 7, 10, and 13th week of academic calendar | Calendared activity | Calendared activity |
| **Topics Covered** | Quiz 1 (L 1--5& T 1) **(CO1)** | Test 1  (L 1-16& T 1-5)  **(CO1-CO3)** | Comprehensive examination covering full syllabus. Students are expected to answer all questions **(CO1-CO5)** |
| Quiz 2 (L **6-12**& T 2-4) **(CO1-CO2)** |
| Quiz 3 (L 13-22& T 5-7) **(CO3)** | Test 2  (L 17-27& T 6-9)  **(CO3-CO4)** |
| Quiz 4 (L 23-32& T 8-10) **(CO4-CO5)** |

**Lesson Plan**

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| **L. No.** | **Topics** | **Course Outcome Addressed** |
| **L0** | INTRODUCTION TO THE COURSE | CO |
| **L1** | BASIC STRUCTURE OF COMPUTERS: COMPUTER TYPES, FUNCTIONAL UNITS | CO1 |
| **L2** | BASIC OPERATIONAL CONCEPTS, NUMBER REPRESENTATION AND ARITHMETIC OPERATIONS | CO1 |
| **L3** | ARITHMETIC OPERATIONS (COND..) | CO1 |
| **T1** | Tutorial 1 on Number representation and Arithmetic Operations | CO1 |
| **L4** | ARITHMETIC OPERATIONS (COND..), CHARACTER REPRESENTATION, PERFORMANCE, SOLVED PROBLEM | CO1 |
| **L5** | FLOATING POINT REPRESENTATION, IEEE STANDARD FLOATING POINT REPRESENTATION, FLOATING POINT ARITHMETIC | CO2 |
| **L6** | INSTRUCTION SET ARCHITECTURE: MEMORY LOCATIONS AND ADDRESSES, MEMORY OPERATIONS | CO1 |
| **T2** | Tutorial 2 on Floating point arithmetic, Memory addressing | CO1 |
| **L7** | INSTRUCTIONS AND INSTRUCTION SEQUENCING, ADDRESSING MODES | CO1 |
| **L8** | CISC INSTRUCTION SETS, RISC AND CISC STYLES, EXAMPLE PROGRAMS, SOLVED PROBLEMS | CO1 |
| **L9** | ARITHMETIC AND LOGIC UNIT: HARDWARE FOR ADDITION AND SUBTRACTION | CO2 |
| **T3** | Tutorial 3 on Addressing modes, RISC and CISC | CO2 |
| **L10** | MULTIPLICATION, HARDWARE IMPLEMENTATION | CO2 |
| **L11** | MULTIPLICATION, HARDWARE IMPLEMENTATION (Contd..) | CO2 |
| **L12** | BOOTH’S ALGORITHM | CO2 |
| **T4** | Tutorial 4 on Addition, Subtraction and Multiplication in ALU | CO2 |
| **L13** | DIVISION | CO2 |
| **L14** | CONTROL UNIT: BASIC CONCEPTS-REGISTER TRANSFER NOTATION, HARDWARE IMPLEMENTATION, BASIC RWM UNIT, BUSES-BIDIRECTIONAL, SINGLE BUS, 2 BUS, 3 BUS ORGANIZATION | CO3 |
| **L15** | DESIGN METHODS-COMPARISON OF HARDWIRED AND MICROPROGRAMMED APPROACH, HARDWIRED CONTROL DESIGN-BOOTHS MULTIPLIER DESIGN | CO3 |
| **T5** | Tutorial 5 on Booth’s Algorithm and Division, Control Design | CO3 |
| **L16** | PROCESSING SECTION DESIGN OF BOOTHS MULTIPLIER | CO3 |
| **L17** | BOOTHS MULTIPLIER CONTROLLER | CO3 |
| **L18** | SEQUENCE COTROLLER DESIGN | CO3 |
| **T6** | Tutorial 6 on Control Unit Design | CO3 |
| **L19** | PLA CONTROL UNIT ORGANIZATION OF BOOTH MULTIPLIER | CO3 |
| **L20** | MICROPROGRAMMED CONTROL UNIT:WILKIE’S DESIGN, MICROPROGRAMMED CONTROL ORGANIZATION | CO3 |
| **L21** | MICROPROGRAMMED MULTIPLIER CONTROL UNIT FOR BOOTHS MULTIPLIER, EXAMPLE ON CONTROL UNIT DESIGN | CO3 |
| **T7** | Tutorial 7 on PLA control unit, Microprogrammed Control Unit | CO3 |
| **L22** | MEMORY SYSTEMS: BASIC CONCEPTS, RAM MEMORIES, INTERNAL ORGANIZATION OF MEMORY CHIPS, STATIC MEMORIES | CO4 |
| **L23** | STRUCTURE OF LARGER MEMORIES, READ-ONLY MEMORIES, MEMORY HIERARCHY | CO4 |
| **L24** | CACHE MEMORIES- MAPPING FUNCTIONS | CO4 |
| **T8** | Tutorial 8 on Larger Memory design, Cache Mapping | CO4 |
| **L25** | PLACEMENT STRATEGIES, REPLACEMENT ALGORITHMS,EXAMPLE OF MAPPING TECHNIQUES | CO4 |
| **L26** | PERFORMANCE CONSIDERATIONS, HIT RATE AND MISS PENALTY, CACHES ON THE PROCESSOR CHIP | CO4 |
| **L27** | VIRTUAL MEMORY, ADDRESS TRANSLATION | CO4 |
| **T9** | Tutorial 9 on Performance of a computer, Address translation | CO4 |
| **L28** | MAGNETIC HARD DISKS | CO4 |
| **L29** | INPUT/OUTPUT ORGANIZATION: ACCESSING I/O DEVICES, I/O DEVICE INTERFACE, PROGRAM-CONTROLLED I/O, INTERRUPTS, ENABLING AND DISABLING INTERRUPTS | CO5 |
| **L30** | HANDLING MULTIPLE DEVICES, CONTROLLING I/O DEVICE BEHAVIOR, PROCESSOR CONTROL REGISTERS, DMA | CO5 |
| **T10** | Tutorial 10 on Interrupts | CO5 |
| **L31** | INTRODUCTION TO PARALLEL ARCHITECTURE: PIPELINING CONCEPTS, PIPELINE ORGANIZATION, ISSUES, DATA DEPENDENCIES | CO5 |
| **L32** | OPERAND FORWARDING, HANDLING DATA DEPENDENCIES IN SOFTWARE, MEMORY DELAYS | CO5 |
| **L33** | BRANCH DELAYS, UNCONDITIONAL BRANCHES, CONDITIONAL BRANCHES, BRANCH DELAY SLOT | CO5 |
| **T11** | Tutorial 11 on Data Dependencies, Branching and Pipelining | CO5 |
| **L34** | HARDWARE MULTITHREADING, VECTOR (SIMD) PROCESSING | CO5 |
| **L35** | GRAPHICS PROCESSING UNITS (GPUs), SHARED MEMORY MULTIPROCESSORS, INTERCONNECTION NETWORKS | CO5 |
| **L36** | CACHE COHERENCE, WRITE-THROUGH PROTOCOL, WRITE-BACK PROTOCOL, SNOOPY CACHES, DIRECTORY BASED CACHE COHERENCE | CO5 |
| **T12** | Tutorial 12 on multithreading, SIMD, Multiprocessors, Cache coherence | CO5 |
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**References:**

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| 1. | Carl Hamacher, ZvonkoVranesic and SafwatZaky, “Computer Organization and Embedded Systems”, Sixth edition, McGraw Hill Publication, 2012. |
| 2. | William Stallings, “Computer Organization and Architecture – Designing for Performance”, 9th edition, PHI, 2015. |
| 3. | Mohammed Rafiquzzaman and Rajan Chandra, “Modern Computer Architecture”, Galgotia Publications Pvt. Ltd., 2010. |
| 4. | D.A. Patterson and J.L.Hennessy, "Computer Organization and Design-The Hardware/Software Interface", Fifth Edition, Morgan Kaufmann, 2014. |
| 5. | J.P.Hayes, "Computer Architecture and Organization", McGraw Hill Publication, 1998. |
| 6. | Click or tap here to enter text. |
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| **Submitted by:** | **Dr. N GOPALAKRISHNA KINI** |

**(Signature of the faculty)**

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| **Date:** | **26-07-2019** |

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| **Approved by:** | **Dr. ASHAlatha Nayak** |

**(Signature of HOD)**

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| **Date:** | **27-07-2019** |

**Faculty members teaching the course (IF MULTIPLE sections EXIST):**

|  |  |  |  |
| --- | --- | --- | --- |
| **FACULTY** | **Section** | **FACULTY** | **Section** |
| Dr. Renuka A (ARN) | A |  |  |
| Ms. Vidya Pai (VP) | B |  |  |
| Dr. N. Gopalakrishna Kini (NGK) | C |  |  |
| Dr. Renuka A (ARN) | D |  |  |
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